

The diagram illustrates a differential signal processing circuit. A dashed box 10 encloses the core differential pair consisting of transistors 11 and 12, which share a common tail current source 15. The gates of transistors 11 and 12 are driven by an AC voltage source 19 through a network of input transistors 13 and 14. The differential outputs of the pair are connected to the non-inverting input (+) of op-amp 17 and the inverting input (-) of op-amp 18. The op-amps are configured with feedback paths to their respective outputs. Below the circuit, a timing diagram 30 shows two frequency components, f_1 and f_2 , with phase shifts of 0° and 180° indicated at specific points. A block 20 is positioned below the timing diagram.

FIG. 1

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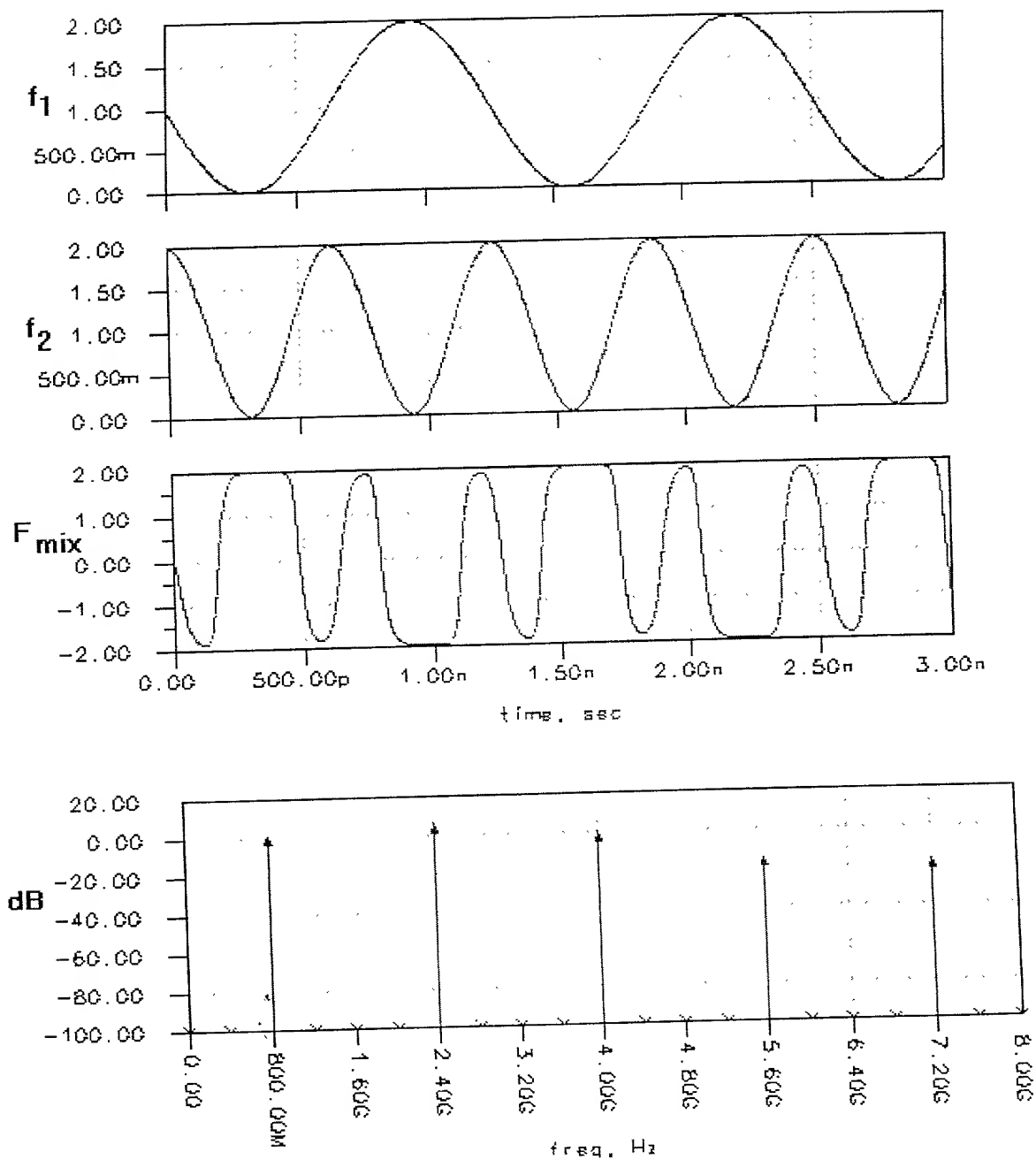


FIG. 2

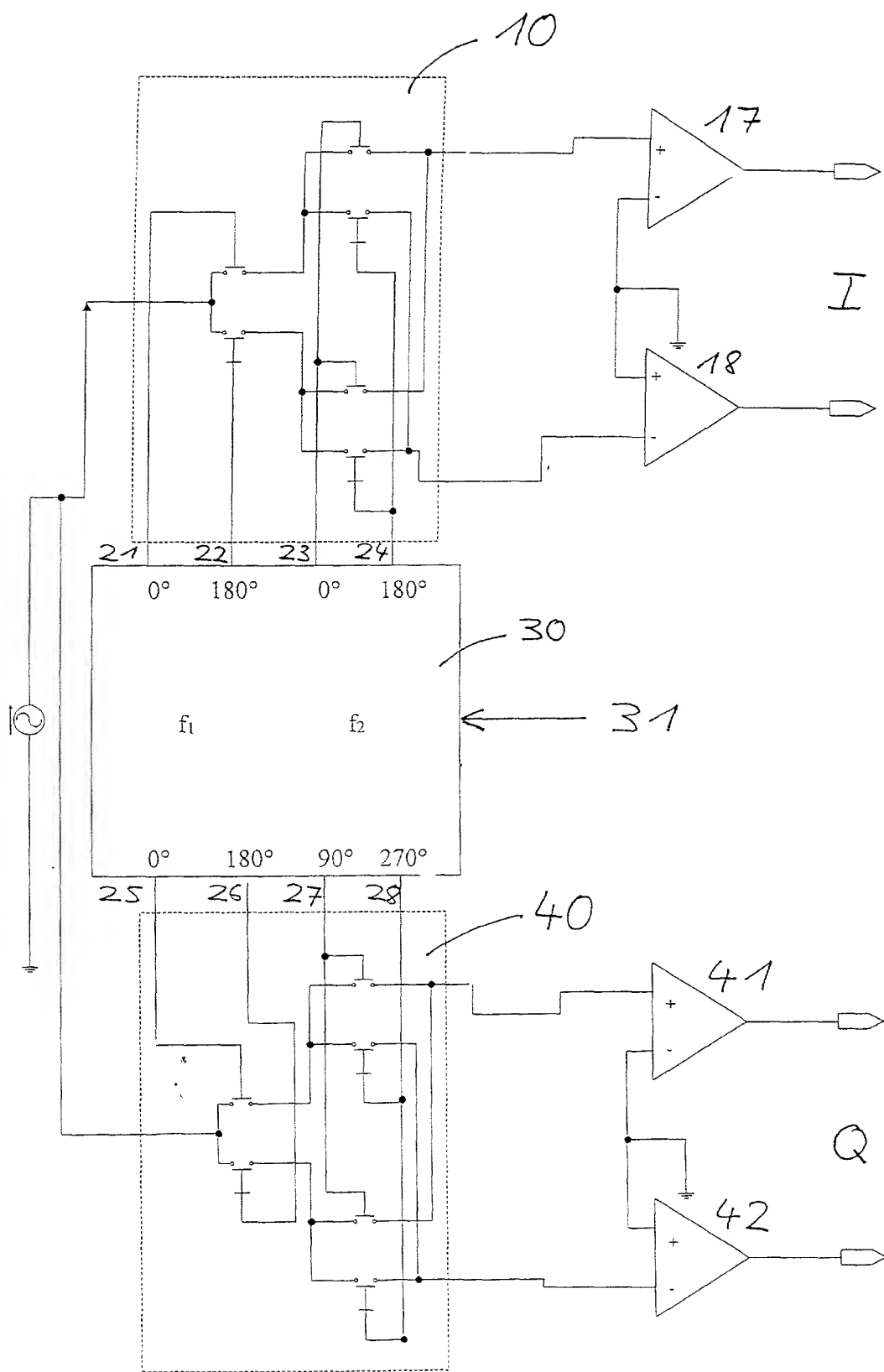


FIG. 3

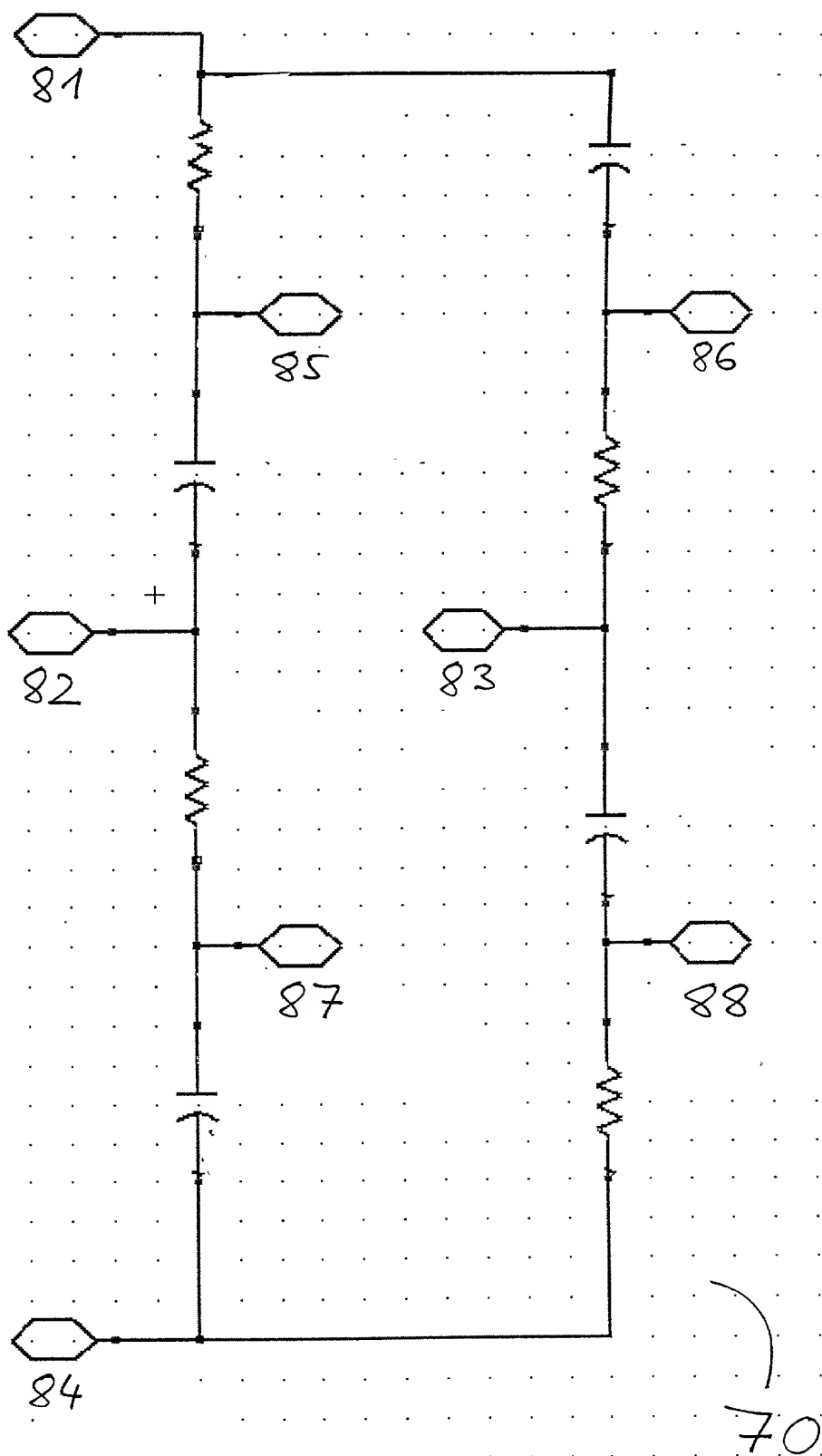


FIG. 4

